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=> s (MOSFET? or FET? or field-effect-transistor? or MISFET?)

         14981 MOSFET?
         65968 FET?
       1224668 FIELD
       1023540 EFFECT
        166921 TRANSISTOR?
         36296 FIELD-EFFECT-TRANSISTOR?
                 (FIELD(W)EFFECT(W)TRANSISTOR?)
           901 MISFET?
L1       92407 (MOSFET? OR FET? OR FIELD-EFFECT-TRANSISTOR? OR MISFET?)

=> s l1 and ((SiC or silicon-carbide?)(5w)gate? or gate?(5w)(SiC or
silicon-carbide?))

         13131 SIC
        201198 SILICON
         68132 CARBIDE?
         22673 SILICON-CARBIDE?
                 (SILICON(W)CARBIDE?)
        236123 GATE?
            88 (SIC OR SILICON-CARBIDE?)(5W)GATE?
        236123 GATE?
         13131 SIC
        201198 SILICON
         68132 CARBIDE?
         22673 SILICON-CARBIDE?
                 (SILICON(W)CARBIDE?)
            83 GATE?(5W)(SIC OR SILICON-CARBIDE?)
L2          86 L1 AND ((SIC OR SILICON-CARBIDE?)(5W)GATE? OR GATE?(5W)(SIC
 OR
                SILICON-CARBIDE?))

=> s l2 and source? and drain?

        805823 SOURCE?
        175302 DRAIN?
L3          80 L2 AND SOURCE? AND DRAIN?

=> d l3 1-80 cit


1.  5,886,368, Mar. 23, 1999, Transistor with silicon oxycarbide gate and
methods of fabrication and use; Leonard Forbes, et al., 257/77, 316, 412
[IMAGE AVAILABLE]

2.  5,885,860, Mar. 23, 1999, Silicon carbide transistor and method;
Charles E. Weitzel, et al., 438/179, 182, 931 [IMAGE AVAILABLE]

3.  5,877,041, Mar. 2, 1999, Self-aligned power field effect
transistor in silicon carbide; Robert T. Fuller, 438/105, 268, 305,
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590, 931 [IMAGE AVAILABLE]

4. 5,849,620, Dec. 15, 1998, Method for producing a semiconductor device comprising an implantation step; Christopher Harris, et al., 438/273, 285 [IMAGE AVAILABLE]

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13. 5,776,837, Jul. 7, 1998, Method of obtaining high quality silicon dioxide passivation on silicon carbide and resulting passivated structures; John W. Palmour, 438/767, 779, 931 [IMAGE AVAILABLE]

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17. 5,742,076, Apr. 21, 1998, Silicon carbide switching devices having near ideal breakdown voltage capability and ultralow on-state resistance; Srikant Sridevan, et al., 257/77, 78, 289, 295, 331, 341, 410 [IMAGE AVAILABLE]

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19. 5,734,180, Mar. 31, 1998, High-performance high-voltage device structures; Satwinder Malhi, 257/77, 339, 347, 506 [IMAGE AVAILABLE]

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AVAILABLE]

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62. 5,323,040, Jun. 21, 1994, Silicon carbide field effect device; Bantval J. Baliga, 257/332, 77, 331, 334, 344 [IMAGE AVAILABLE]

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71. 5,135,885, Aug. 4, 1992, Method of manufacturing silicon carbide **FETS**; Katsuki Furukawa, et al., 438/167, 285, 522, 931 [IMAGE AVAILABLE]

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US PAT NO: 5,886,368 [IMAGE AVAILABLE] L3: 1 of 80

ABSTRACT:
A CMOS-compatible **FET** has a reduced electron affinity polycrystalline or microcrystalline silicon oxycarbide (SiOC) gate that is electrically isolated (floating) or interconnected. The SiOC material composition is selected to establish a desired barrier energy between the SiOC gate and a gate insulator. In a memory application, such as a flash EEPROM, the SiOC composition is selected to establish a lower barrier energy to reduce write and erase voltages and times or accommodate the particular data charge retention time needed for the particular application. In a light detector or imaging application, the SiOC composition is selected to provide sensitivity to the desired wavelength of light. Unlike conventional photodetectors, light is absorbed in the floating gate, thereby ejecting previously stored electrons therefrom. Also unlike conventional photodetectors, the light detector according to the present invention is actually more sensitive to lower energy photons as the semiconductor bandgap is increased.

US PAT NO: 5,885,860 [IMAGE AVAILABLE] L3: 2 of 80

ABSTRACT:
A silicon carbide MESFET (10) is formed to have a **source** (21) and a **drain** (22) that are self-aligned to a gate (16) of the MESFET (10). The gate (16) is formed to have a T-shaped structure with a gate-to-**source** spacer (18) and gate-to-**drain** spacer (19) along each side of a base of the gate (16). The gate (16) is used as a mask for implanting dopants to form the **source** (21) and **drain** (22). A laser annealing is performed after the implantation to activate the

dopants. Because the laser annealing is a low temperature operation, the gate (16) is not detri[redacted]tally affected during the anne[redacted]g.

US PAT NO: 5,877,041 [IMAGE AVAILABLE] L3: 3 of 80

ABSTRACT:
The present invention is directed to a silicon carbide **field effect transistor**. The **FET** is formed on a **silicon carbide** monocrystalline substrate. An insulative material **gate** having a pair of spaced apart sidewalls is patterned on the substrate. The insulative material comprises a first insulation material overlayed by an electrically conductive layer. Within the substrate is lightly doped base regions located partially under the sidewalls of the gate and extending into the exposed substrate. Associated with the lightly doped base regions are heavily doped **source** regions aligned with the exposed substrate. On the underside of the substrate is a **drain** region to form the **FET**. Further in accordance with the present invention, a method to fabricate a **field effect transistor** is disclosed. The transistor is formed in a monocrystalline substrate of silicon carbide. Forming a transistor on the silicon carbide substrate entails depositing a first electrically insulative layer over the substrate. Next, an electrically conductive layer is deposited over the first insulative layer and then a second electrically insulative layer is deposited over the conductive layer. The following step includes partially removing the second insulative layer and exposing a portion of the first conductive layer to obtain two spaced apart regions of the silicon carbide substrate for forming lightly doped base regions. Then the substrate aligned with the exposed portion of the first conductive layer is lightly implanted with a dopant to form lightly doped base regions. Next, a layer of a third insulative material is formed on the sidewalls of the second insulative material. The following step entails removing the exposed conductive layer not aligned with the second insulative material and third insulative material. Thereby, exposing portions of the first insulating layer and defining a second set of spaced regions of the substrate. The second set of spaced regions are then heavily implanted to form heavily doped **source** regions. The second insulative material and third insulative material are then removed to form a gate.

US PAT NO: 5,849,620 [IMAGE AVAILABLE] L3: 4 of 80

ABSTRACT:
A method for producing a semiconductor device having a semiconductor layer of SiC is disclosed. The method comprises the steps of applying an insulation layer on the semiconductor layer, implanting first impurity dopant into the semiconductor layer, and annealing this layer at at least about 1500.degree. C. so that the implanted first impurity dopant is activated, wherein the insulating layer comprises AlN as a major component and the insulating layer is applied before the annealing step and maintained on the semiconductor layer during the annealing step.

US PAT NO: 5,831,292 [IMAGE AVAILABLE] L3: 5 of 80

ABSTRACT:
A transistor of **SiC** having an insulated **gate** comprises a **drain** contact with a highly doped substrate layer formed on the **drain**. The substrate layer is of p-type or of n-type. For a p-type transistor, a highly doped n-type buffer layer may optionally be formed on top of the substrate layer. A low doped n-type drift layer, a highly doped p-type base layer, a highly doped n-type **source** region, and a **source** contact are then superimposed on the substrate layer. A vertical trench extends through the **source** region and the base layer to at least the drift layer. The trench has a wall next to these layers. A gate electrode extends vertically along the wall and at least over a vertical extension of the base layer. An insulating layer is arranged

between the gate electrode and at least the base layer whereby an inversion channel is formed for electron transport from the **source** contact to the **drain** contact. An additional low doped p-type layer is arranged in the channel region laterally to the base layer, between the base layer and the insulating layer. The additional layer extends vertically over at least the base layer.

US PAT NO: 5,831,289 [IMAGE AVAILABLE] L3: 6 of 80

ABSTRACT:
A **silicon carbide gate** turn off thyristor (GTO) has a silicon carbide junction **field effect transistor** (JFET) connected between the gate of the GTO and one of its anode or cathode electrodes thereby minimizing cooling requirements while providing for rapid switching.

US PAT NO: 5,831,288 [IMAGE AVAILABLE] L3: 7 of 80

ABSTRACT:
A silicon carbide (SiC) metal-insulator semiconductor **field effect transistor** having a u-shaped **gate** trench and an n-type **SiC** drift layer is provided. A p-type region is formed in the SiC drift layer and extends below the bottom of the u-shaped gate trench to prevent field crowding at the corner of the gate trench. A unit cell of a metal-insulator semiconductor transistor is provided having a bulk single crystal SiC substrate of n-type conductivity SiC, a first epitaxial layer of n-type SiC and a second epitaxial layer of p-type SiC. First and second trenches extend downward through the second epitaxial layer and into the first epitaxial layer with a region of n-type SiC between the trenches. An insulator layer is formed in the first trench with the upper surface of the insulator on the bottom of the trench below the second epitaxial layer. A region of p-type SiC is formed in the first epitaxial layer below the second trench. Gate and **source** contacts are formed in the first and second trenches respectively and a **drain** contact is formed on the substrate.

US PAT NO: 5,828,101 [IMAGE AVAILABLE] L3: 8 of 80

ABSTRACT:
A semiconductor device has trenches formed on the surface of a semiconductor. The device passes a main current through a channel formed between the trenches and controls the main current with the use of gate electrodes buried in the trenches. The main current directly controlled by the gate electrodes flows in parallel with the surface of the semiconductor and is distributed vertically to the surface of the semiconductor. The width W of the channel is freely increased without regard to the surface area of the semiconductor.

US PAT NO: 5,821,576 [IMAGE AVAILABLE] L3: 9 of 80

ABSTRACT:
The invention provides for a **field effect transistor** (**FET**) which includes a substrate and a buffer layer formed upon the substrate and an active layer formed upon the buffer layer. The active layer includes a gate region, **drain** region and **source** region. In addition, a channel region is formed in the active layer intermediate the **source** region and **drain** region. The channel region includes a first portion of reduced thickness adjacent the **drain** region. The active layer may include a recess adjacent the **drain** region to provide the thin channel region. Preferably, the thickness of the first portion of the channel region is equal to the undepleted channel thickness within the second portion of the channel region adjacent the first portion. The substrate, buffer layer, active layer, and degenerate layers are preferably fabricated of silicon carbide or gallium nitride. Further, the **FET** preferably includes a p type buffer, n type active

layer, and n+ degenerate layers. The **FET** may also include a surface-effect-suppressive layer which preferably covers portions of the active layer and the degenerate layers.

US PAT NO: 5,801,401 [IMAGE AVAILABLE] L3: 10 of 80

ABSTRACT:
A memory is described which has memory cells that store data using hot electron injection. The data is erased through electron tunneling. The memory cells are described as floating gate transistors wherein the floating gate is fabricated using a conductive layer of microcrystalline silicon carbide particles. The microcrystalline silicon carbide particles are in contact such that a charge stored on the floating gate is shared between the particles. The floating gate has a reduced electron affinity to allow for data erase operations using lower voltages.

US PAT NO: 5,798,548 [IMAGE AVAILABLE] L3: 11 of 80

ABSTRACT:
A semiconductor device includes a semiconductor substrate, **source** and **drain** regions defined in the semiconductor substrate with a channel region therebetween, a first insulating layer located over the semiconductor substrate including over the channel region, a floating gate locating over the first insulating layer, a second insulating layer located over the floating gate, a first control gate located over the second insulating layer, a third insulating layer located over the first control gate, a second control gate located over the third insulating layer. The first and second control gates allow the injection of hot carriers onto the floating gate from the first control gate when predetermined first and second voltages are applied to the first and second control gates, respectively.

US PAT NO: 5,780,878 [IMAGE AVAILABLE] L3: 12 of 80

ABSTRACT:
A lateral gate, vertical drift region transistor including a **drain** positioned on one surface of a substrate and a doped structure having a buried region therein positioned on the other surface of the substrate. The buried region defining a drift region in the doped structure extending vertically from the substrate and further defining a doped region in communication with the drift region and adjacent the surface of the doped structure. A **source** positioned on the doped structure in communication with the doped region. An insulating layer positioned on the doped structure with a metal gate positioned on the insulating layer so as to define an accumulation region extending laterally adjacent the control terminal and communicating with the drift region and the **source**.

US PAT NO: 5,776,837 [IMAGE AVAILABLE] L3: 13 of 80

ABSTRACT:
A method of obtaining high quality passivation layers on silicon carbide surfaces by oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer on the silicon carbide portion that is substantially free of dopants that would otherwise degrade the electrical integrity of the oxide layer.

US PAT NO: 5,753,938 [IMAGE AVAILABLE] L3: 14 of 80

ABSTRACT:
A semiconductor switching device includes a plurality of adjacent heterojunction-gate static-induction transistor (SIT) unit cells connected in parallel in a monocrystalline silicon carbide substrate

having first and second opposing faces, a relatively highly doped silicon carbide **drain** region adjacent the first face and a relatively highly doped silicon carbide **source** region adjacent the second face. A relatively lightly doped drift region is also provided in the substrate and extends between the **drain** region and **source** region. A plurality of trenches are also provided in the substrate so that sidewalls of the trenches extend adjacent the drift region. Each trench preferably contains a relatively highly doped second conductivity type nonmonocrystalline silicon gate region comprised of a material selected from the group consisting of polycrystalline silicon or amorphous silicon. These gate regions form P-N heterojunctions with the drift region at the sidewalls and bottoms of the trenches. An electrically insulating layer, such as a thermally grown silicon dioxide layer, is also provided on the nonmonocrystalline silicon gate regions in order to electrically insulate the gate regions from metallization on the second face. The use of nonmonocrystalline materials for the gate regions is preferred because the nonmonocrystalline lattice structure of the gate regions provides numerous grain boundaries and other lattice defects which act as scattering sites for electrons. By providing scattering sites, the probability that accelerated electrons will reach the threshold energy to induce avalanche breakdown in the gate regions is reduced and an increase in forward blocking voltage capability is achieved. Hole injection from the P+ polycrystalline silicon gate region into the N-type drift can also be suppressed to significantly improve the switching speed by reducing the amount of stored charge in the drift region.

US PAT NO: 5,747,831 [IMAGE AVAILABLE] L3: 15 of 80

ABSTRACT:

SiC field-effect transistors with **source**, **gate** and **drain** contacts and in which the **source** contacts are located on the surface of the semiconductor wafer, the **drain** contacts on the underside of the wafer and the gate contacts in trench-like structures. The trench-like structures surround the **source** electrodes of the transistors in the shape of a ring and the gate contacts are connected to each other on the floors of the trenches.

US PAT NO: 5,744,826 [IMAGE AVAILABLE] L3: 16 of 80

ABSTRACT:
A semiconductor substrate 4 consisting of an n.sup.+ -type substrate 1, an n.sup.- -type silicon carbide semiconductor layer 2 and a p-type silicon carbide semiconductor layer 3, made of hexagonal crystal-based single crystal silicon carbide with the main surface having a planar orientation approximately in the (0001) carbon face. An n.sup.+ -type **source** region 5 is formed in the surface layer of the semiconductor layer 3, and a trench 7 runs from the main surface through the region 5 and the semiconductor layer 3 reaching to the semiconductor layer 2, and extending approximately in the [1120] direction. An n-type silicon carbide semiconductor thin-film layer 8 is provided on the region 5, the semiconductor layer 3 and the semiconductor layer 2 on the side walls of the trench 7, while a gate electrode layer 10 is formed on the inner side of a gate insulating film 9, a **source** electrode layer 12 is formed on the surface of the semiconductor region 5, and a **drain** electrode layer 13 is formed on the surface of the n.sup.+ -type substrate 1.

US PAT NO: 5,742,076 [IMAGE AVAILABLE] L3: 17 of 80

ABSTRACT:
A silicon carbide switching device having near ideal electrical characteristics includes an electrical insulator with an electrical permittivity greater than about ten times the permittivity of free space (.epsilon..sub.o) and more preferably greater than about fifteen times

the permittivity of free space, as a gate electrode insulating region. The use of electrical insulators having high electrical permittivities relative to conventional electrical insulators such as silicon dioxide significantly improves the breakdown voltage and on-state resistance characteristics of a silicon carbide switching device to the point of near ideal characteristics, as predicted by theoretical analysis. Thus, the preferred advantages of using silicon carbide, instead of silicon, can be more fully realized. Electrical insulators having low critical electric field strengths relative to conventional electrical insulators such as silicon dioxide can also be used even though these insulators are relatively more susceptible to field induced dielectric breakdown for a given electric field strength. Such electrical insulators include titanium dioxide.

US PAT NO: 5,736,753 [IMAGE AVAILABLE] L3: 18 of 80

ABSTRACT:
To provide a **field-effect transistor** having a large power conversion capacity and its fabrication method by decreasing the leakage current between the **source** and the **drain** of a semiconductor device made of hexagonal-system **silicon carbide** when the **gate** voltage of the semiconductor device is turned off and also decreasing the electrical resistance of the semiconductor device when the gate voltage of the semiconductor device is turned on. The main current path of the **field-effect transistor** is formed so that the current flowing between the **source** and the **drain** of, for example, a **field-effect transistor** flows in the direction parallel with the {0001} plane and a channel forming plane is parallel with the {1120} plane. [Selected Drawing]FIG. 1

US PAT NO: 5,734,180 [IMAGE AVAILABLE] L3: 19 of 80

ABSTRACT:
An improved high-voltage device structure (10, 50, or 60) is a hybrid silicon-based/non-silicon-based power device that has a low R.sub.ds(on) relative to devices formed using only a silicon substrate and includes control circuit (14, 14', or 14") formed on silicon substrate region (12 or 62). High-voltage circuit (16, 16' or 16") is formed in non-silicon substrate region (18). Connecting circuitry (34 and 66) connects control circuit (14, 14', and 14") with high-voltage circuit (16, 16' or 16") to form high-voltage device structure (10, 50 or 60) that has improved control circuit performance and improved high-voltage circuits performance over devices formed solely from a silicon substrate or solely from a non-silicon substrate.

US PAT NO: 5,731,690 [IMAGE AVAILABLE] L3: 20 of 80

ABSTRACT:
In an electric power supply system including an alternator generating a low-voltage for energizing a battery and a low-voltage load and a high-voltage for energizing a high-voltage load such as a heater for a catalytic converter. Switching elements are disposed in an alternator housing to supply a low-voltage load and a high-voltage load selectively. The switching elements compose a part of rectifying unit for supplying DC output power to the high-voltage or low-voltage load.

US PAT NO: 5,726,558 [IMAGE AVAILABLE] L3: 21 of 80

ABSTRACT:
Reverse current is supplied from a battery to armature coils of a three-phase synchronous power generator, via semiconductor switching devices of a three-phase full-wave rectifier, by controlling the switches. By this control, the reverse current will reduce waveform distortion of armature current of each phase so as to reduce the electromagnetic force pulsation and, therefore, reduce vibration or

noise.

US PAT NO: 5,726,557 [IMAGE AVAILABLE] L3: 22 of 80

ABSTRACT:
A vehicular electric power system is composed of a rotating AC machine having polyphase armature coils, a full-wave rectifier for rectifying the generated voltages by a plurality of SiC-**MOSFETs** to give a rectified output to the battery unit, and a control device for selectively turning on the plurality of SiC-**MOSFETs** to raise the generated voltages by short-circuiting and open-circuiting the armature coils on the basis of the phases of voltages generated by the rotating AC machine at a predetermined duty factor.

US PAT NO: 5,726,463 [IMAGE AVAILABLE] L3: 23 of 80

ABSTRACT:
A **SiC MOSFET** having a self-aligned **gate** structure is fabricated upon a monocrystalline substrate layer, such as a p type conductivity .alpha.6H silicon carbide (SiC) substrate. An SiC n+ type conductivity layer, epitaxially grown on the substrate layer, includes a steep-walled groove etched through the n+ SiC layer and partially into the p SiC layer. The groove is lined with a thin layer of silicon dioxide which extends onto the n+ type conductivity layer. A filling of gate metal over the layer of silicon dioxide is contained entirely in the groove. The silicon dioxide layer includes a first window extending to the filling of gate metal in the groove, and second and third windows extending to the n+ type conductivity layer on either side of the groove, respectively. A gate contact extends through the first window to the filling of gate metal in the groove while **drain** and **source** contacts extend through the second and third window, respectively, to make contact with the n+ type conductivity layer in **drain** and **source** regions on either side of the groove.

US PAT NO: 5,719,410 [IMAGE AVAILABLE] L3: 24 of 80

ABSTRACT:
A **MOSFET** in which the gate electrode is formed of a polycrystalline silicon film, a silicon nitride film having a nitrogen surface density of lens than 8.times.10.sup.14 cm.sup.-2, and a tungsten film--these films formed one upon another in the order mentioned. The gate electrode thus formed, serves to shorten the delay time of the **MOSFET**.

US PAT NO: 5,719,409 [IMAGE AVAILABLE] L3: 25 of 80

ABSTRACT:
A silicon carbide (SIC) metal-insulator semiconductor **field effect transistor** having a u-shaped **gate** trench and an n-type **SiC** drift layer is provided. A p-type region is formed in the SiC drift layer and extends below the bottom of the u-shaped gate trench to prevent field crowding at the corner of the gate trench. A unit cell of a metal-insulator semiconductor transistor is provided having a bulk single crystal SiC substrate of n-type conductivity SiC, a first epitaxial layer of n-type SiC and a second epitaxial layer of p-type SiC. First and second trenches extend downward through the second epitaxial layer and into the first epitaxial layer with a region of n-type SiC between the trenches. An insulator layer is formed in the first trench with the upper surface of the insulator on the bottom of the trench below the second epitaxial layer. A region of p-type SiC is formed in the first epitaxial layer below the second trench. Gate and **source** contacts are formed in the first and second trenches respectively and a **drain** contact is formed on the substrate.

US PAT NO: 5,710,455 [IMAGE AVAILABLE] L3: 26 of 80

ABSTRACT:
A **FET** including a channel region and a drift region in a channel layer with a **source** in the channel region and a **drain** in the drift region. The current channel between the **source** and **drain** defining a straight transistor portion and a curved transistor portion. An oxide with a thin portion overlying the channel region and a thick portion overlying the drift region, and a gate on the thin oxide overlying the current channel. A **drain** field plate and a gate field plate on the thick oxide with spaced apart edges and a damaged region underlying the edges of the field plates only in the curved transistor portion to reduce electric fields at the edges of the field plates. Also, the current channel has a greater length and the edges are spaced apart farther in the curved transistor portions.

US PAT NO: 5,698,771 [IMAGE AVAILABLE] L3: 27 of 80

ABSTRACT:
A hydrocarbon gas detection device operates by dissociating or electro-chemically oxidizing hydrocarbons adsorbed to a silicon carbide detection layer. Dissociation or oxidation are driven by a varying potential applied to the detection layer. Different hydrocarbon species undergo reaction at different applied potentials so that the device is able to discriminate among various hydrocarbon species. The device can operate at temperatures between 100.degree. C. and at least 650.degree. C., allowing hydrocarbon detection in hot exhaust gases. The dissociation reaction is detected either as a change in a capacitor or, preferably, as a change of current flow through an **FET** which incorporates the silicon carbide detection layers. The silicon carbide detection layer can be augmented with a pad of catalytic material which provides a signal without an applied potential. Comparisons between the catalytically produced signal and the varying potential produced signal may further help identify the hydrocarbon present.

US PAT NO: 5,696,396 [IMAGE AVAILABLE] L3: 28 of 80

ABSTRACT:
A vertical **MOSFET**, which can control AC current flowing through a device only by the gate voltage, is obtained. On an n.sup.+ silicon layer is formed an n.sup.- silicon layer. Within the n.sup.- silicon layer is formed a p-body region. Within the p-body region is formed an n.sup.+ **source** region. On top of a substrate are formed a **source** electrode in contact only with the **source** region and a base electrode in contact only with the p-body region. The **source** electrode and the base electrode are connected to each other through a resistance at the outside. On a channel region is formed a gate electrode through a gate oxide film (insulating film). When the above semiconductor device is in the reverse bias conduction, the exciting current is controlled only by the gate voltage by setting the current flowing from a **source** terminal through the resistance to the base electrode, the p-body region and the n.sup.- silicon layer to be negligibly small as compared with the current flowing from the **source** terminal through the **source** electrode to the n.sup.+ **source** region, the channel region and the n.sup.- silicon layer.

US PAT NO: 5,694,311 [IMAGE AVAILABLE] L3: 29 of 80

ABSTRACT:
A power supply system has a three-phase alternating current generator, a storage battery, and a three-phase rectifying device connected between the alternating current generator and the storage battery. The rectifying device includes three SiC-**MOSFETS** which are turned on when the corresponding alternating voltage is positive and turned off when the corresponding alternating voltage is negative. A duty control device switches each of the three SiC-**MOSFETS** on and off according to a selected duty ratio so that the alternating current generator can

generate an optimum voltage in proportion to a rotational speed of a rotor of the alternating current generator.

US PAT NO: 5,693,569 [IMAGE AVAILABLE] L3: 30 of 80

ABSTRACT:
A silicon carbide trench **MOSFET** is provided that includes a first conductivity type semiconductor substrate made of silicon carbide. A first conductivity type drift layer and a second conductivity type base layer, both made of silicon carbide, are sequentially formed by epitaxial growth on the semiconductor substrate. The first conductivity type drift layer has a lower impurity concentration than the semiconductor substrate. A first conductivity type **source** region is formed in a part of a surface layer of the second conductivity type base layer. A gate electrode is received through an insulating film, in a first trench extending from a surface of the first conductivity type **source** region to reach the first conductivity type drift layer. A Schottky electrode disposed on an inner surface of a second trench having a greater depth than the first trench.

US PAT NO: 5,686,737 [IMAGE AVAILABLE] L3: 31 of 80

ABSTRACT:
A metal-semiconductor **field-effect-transistor** (MESFET) is disclosed that exhibits reduced **source** resistance and higher operating frequencies. The MESFET comprises an epitaxial layer of **silicon carbide**, and a **gate** trench in the epitaxial layer that exposes a **silicon carbide gate** surface between two respective trench edges. A gate contact is made to the gate surface, and with the trench further defines the **source** and **drain** regions of the transistor. Respective ohmic metal layers form ohmic contacts on the **source** and **drain** regions of the epitaxial layer, and the edges of the metal layers at the trench are specifically aligned with the edges of the epitaxial layer at the trench.

US PAT NO: 5,681,762 [IMAGE AVAILABLE] L3: 32 of 80

ABSTRACT:
A silicon carbide semiconductor device includes a silicon carbide substrate, an active layer in the substrate and a silicon carbide buried layer which provides a conduction barrier between the substrate and at least a portion of the active layer. The buried layer is preferably formed by implanting second conductivity type dopants into the substrate so that a P-N junction barrier is provided between the active layer and the substrate. The buried layer may also be formed by implanting electrically inactive ions into the substrate so that a relatively high resistance barrier is provided between the active layer and the substrate. The electrically inactive ions are preferably selected from the group consisting of argon, neon, carbon and silicon, although other ions which are electrically inactive in silicon carbide may be used. The implantation of the electrically inactive ions is designed to cause the formation of a large number of electrically active deep level defects in the buried layer, particularly near the peak of the implant profile which is Gaussian in shape. These steps can be utilized in the formation of a variety of silicon carbide semiconductor devices such as lateral field effect devices and devices having both vertical and lateral active regions which are designed for high power applications. In particular, lateral silicon carbide-on-insulator enhancement and depletion mode **field effect transistors** (**FETs**) can be formed in accordance with the present invention. Vertical silicon carbide power MESFET devices can also be formed by incorporating a silicon carbide **source** region in the active layer at the first face of a silicon carbide substrate and a **drain** region at the second face and by providing a Schottky barrier gate electrode on the first face.

US PAT NO: 5,677,616 [IMAGE AVAILABLE] L3: 33 of 80

ABSTRACT:
In a rectifying and voltage regulating unit of an AC generator, an AC input terminal, a DC output terminal, and an insulating member holding the respective terminals are commonly used by a rectifier and a voltage regulator so that a terminal block of the rectifier, a terminal block of the voltage regulator and a connector can be simultaneously molded in a single resin mold and no specific fastening member is necessary. The environmental resistibility of electrically connecting sections of the rectifier and the voltage regulator is enhanced by keeping the connecting sections from exposure by means of sealing the AC input terminal and the DC output terminal with the insulating member.

US PAT NO: 5,661,312 [IMAGE AVAILABLE] L3: 34 of 80

ABSTRACT:
A silicon carbide **MOSFET** (10) is formed to have a high breakdown voltage. A breakdown enhancement layer (20) is formed between a channel region (14) and a drift layer (12). The breakdown enhancement layer (20) has a lower doping concentration that increases the width of a depletion region (24) near a gate insulator (17). The increased depletion region width improves the breakdown voltage.

US PAT NO: 5,641,695 [IMAGE AVAILABLE] L3: 35 of 80

ABSTRACT:
An implant mask (14) and an etch mask (16) are utilized in forming a silicon carbide JFET (10). A **source** opening (17) and a **drain** opening (18) are formed in the masks (14,16). The etch mask (16) is removed, and a **source** area (19) and a **drain** area 21 are implanted through the openings (17,18) and **source** and **drain** contact (23, 24) are formed. A protective layer (26) is used to form **source** and **drain** contacts (23,24). A gate contact (27) is utilized to ensure the gate (28) is self-aligned to the gate contact (27).

US PAT NO: 5,629,531 [IMAGE AVAILABLE] L3: 36 of 80

ABSTRACT:
A method of obtaining high quality passivation layers on silicon carbide surfaces by oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer on the silicon carbide portion that is substantially free of dopants that would otherwise degrade the electrical integrity of the oxide layer.

US PAT NO: 5,614,749 [IMAGE AVAILABLE] L3: 37 of 80

ABSTRACT:
A silicon carbide trench **MOSFET** is provided that includes a first conductivity type semiconductor substrate made of silicon carbide. A first conductivity type drift layer and a second conductivity type base layer, both made of silicon carbide, are sequentially formed by epitaxial growth on the semiconductor substrate. The first conductivity type drift layer has a lower impurity concentration than the semiconductor substrate. A first conductivity type **source** region is formed in a part of a surface layer of the second conductivity type base layer. A gate electrode is received through an insulating film, in a first trench extending from a surface of the first conductivity type **source** region to reach the first conductivity type drift layer. A Shottky electrode disposed on an inner surface of a second trench having a greater depth than the first trench.

US PAT NO: 5,612,260 [IMAGE AVAILABLE] L3: 38 of 80

ABSTRACT:
A method of obtaining high quality passivation layers on silicon carbide surfaces by oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer on the silicon carbide portion that is substantially free of dopants that would otherwise degrade the electrical integrity of the oxide layer.

US PAT NO: 5,597,744 [IMAGE AVAILABLE] L3: 39 of 80

ABSTRACT:
Electrodes 16a and 16b composed of metal nitride made of either one of TiN, ZrN, HfN, VN and TaN are formed on an N-type **source** region 12 and **drain** region 13 of a P-type SiC substrate 11, respectively, Nitrogen-rich layers 12a and 13a are formed in surface layer portions of the regions 12 and 13 which the electrodes composed of metal nitride 16a and 16b contact respectively. The nitrogen-rich layer allows the contact resistivity of the electrode to be made small, A metal nitride composed of either one of TiN, ZrN, HfN, VN and TaN is interposed between a gate electrode 15 of Mo and an interconnection of Al 17c to prevent the reaction of the gate electrode and the interconnection.

US PAT NO: 5,589,695 [IMAGE AVAILABLE] L3: 40 of 80

ABSTRACT:
An improved high-voltage device structure (10, 50, or 60) is a hybrid silicon-based/non-silicon-based power device that has a low R.sub.ds(on) relative to devices formed using only a silicon substrate and includes control circuit (14, 14' or 14") formed on silicon substrate region (12 or 62). High-voltage circuit (16, 16' or 16") is formed in non-silicon substrate region (18). Connecting circuitry (34 and 66) connects control circuit (14, 14', and 14") with high-voltage circuit (16, 16' or 16") to form high-voltage device structure (10, 50 or 60) that has improved control circuit performance and improved high-voltage circuits performance over devices formed solely from a silicon substrate or solely from a non-silicon substrate.

US PAT NO: 5,574,295 [IMAGE AVAILABLE] L3: 41 of 80

ABSTRACT:
A metal-oxide-semiconductor **field-effect transistor** (**MOSFET**) device comprising a carrier wafer and a silicon gate region disposed on the carrier wafer. A **source** region and a **drain** region made from 3C-silicon carbide are disposed on the carrier wafer above the gate region. A gate oxide, derived from silicon, separates the **source** and **drain** regions from the gate region. Laterally oriented oxide trenches separate and dielectrically isolate the **MOSFET** device from other devices on the carrier wafer. Further, the **MOSFET** device described above is manufactured in a method comprising the steps of providing a carrier wafer having an oxide layer formed on a surface thereof. A layer of silicon having a given level of conductivity is bonded to the oxide layer of the carrier wafer. Selected portions of the layer of silicon are oxidized to create a plurality of dielectrically isolated silicon islands, one of which forms a gate region. A layer of silicon dioxide is then formed over the dielectrically isolated islands of silicon. Two layers of silicon carbide are then bonded to the layer of silicon dioxide. A **source** region and a **drain** region are each formed from the layers of silicon carbide. Selected portions of one of the two layers of silicon carbide are oxidized to dielectrically isolate the **source** region and the **drain** region from other semiconductor devices located on the carrier wafer.

US PAT NO: 5,569,624 [IMAGE AVAILABLE] L3: 42 of 80

ABSTRACT:
A doping sequence that reduces the cost and complexity forming **source/drain** regions in complementary metal oxide silicon (CMOS) integrated circuit technologies. The process combines the use of patterned excimer laser annealing, dopant-saturated spin-on glass, silicide contact structures and interference effects creates by thin dielectric layers to produce **source** and **drain** junctions that are ultrashallow in depth but exhibit low sheet and contact resistance. The process utilizes no photolithography and can be achieved without the use of expensive vacuum equipment. The process margins are wide, and yield loss due to contact of the ultrashallow dopants is eliminated.

US PAT NO: 5,565,692 [IMAGE AVAILABLE] L3: 43 of 80

ABSTRACT:
For protecting the gate insulating layer of an insulated gate **field-effect transistor** from electrostatic charges, the main terminals of a depletion mode (normally conducting) **field-effect transistor**, serving as a protection transistor, are connected between the gate and **source** terminals of the transistor to be protected, thus providing a shunt path for electrostatic charges when the protection transistor is not biased out of conduction. For normal operation, the protection transistor is biased out of conduction by applying to its gate terminal the voltage drop across a biasing resistor in series with the **source** terminal of the insulated gate **field-effect transistor**. This protection arrangement is particularly advantageous for silicon carbide **field-effect transistors** which are not readily suited to application of conventional (i.e. silicon transistor) gate insulating layer protection techniques.

US PAT NO: 5,543,637 [IMAGE AVAILABLE] L3: 44 of 80

ABSTRACT:
A silicon carbide semiconductor device includes a silicon carbide substrate, an active layer in the substrate and a silicon carbide buried layer which provides a conduction barrier between the substrate and at least a portion of the active layer. The buried layer is preferably formed by implanting second conductivity type dopants into the substrate so that a P-N junction barrier is provided between the active layer and the substrate. The buried layer may also be formed by implanting electrically inactive ions into the substrate so that a relatively high resistance barrier is provided between the active layer and the substrate. The electrically inactive ions are preferably selected from the group consisting of argon, neon, carbon and silicon, although other ions which are electrically inactive in silicon carbide may be used. The implantation of the electrically inactive ions is designed to cause the formation of a large number of electrically active deep level defects in the buried layer, particularly near the peak of the implant profile which is Gaussian in shape. These steps can be utilized in the formation of a variety of silicon carbide semiconductor devices such as lateral field effect devices and devices having both vertical and lateral active regions which are designed for high power applications. In particular, lateral silicon carbide-on-insulator enhancement and depletion mode **field effect transistors** (FFTs) can be formed in accordance with the present invention. Vertical silicon carbide power MESFET devices can also be formed by incorporating a silicon carbide **source** region in the active layer at the first face of a silicon carbide substrate and a **drain** region at the second face and by providing a Schottky barrier gate electrode on the first face.

US PAT NO: 5,514,604 [IMAGE AVAILABLE] L3: 45 of 80

ABSTRACT:
A **MOSFET** includes a first SiC semiconductor contact layer, a SiC

semiconductor channel layer supported by the first SiC contact layer, and a second SiC semiconductor contact layer supported by the channel layer. The second contact and channel layers are patterned to form a plurality of gate region grooves therethrough. Each of the gate region grooves includes a base surface and side surfaces which are covered with groove oxide material. A plurality of metal gate layers are provided, each being supported in a respective one of the plurality of grooves. A plurality of deposited oxide layers are provided, each in a respective one of the grooves so as to be supported by a respective one of the plurality of metal gate layers. A first metal contact layer is applied to the surface of the first SiC contact layer, and a second metal contact layer is applied to a portion of the surface of the second SiC contact layer.

US PAT NO: 5,510,632 [IMAGE AVAILABLE] L3: 46 of 80

ABSTRACT:
A silicon carbide (SiC) junction **field effect transistor** (JFET) device is fabricated upon a substrate layer, such as a p type conductivity SiC substrate, using ion implantation for the **source** and **drain** areas. A SiC p type conductivity layer is epitaxially grown on the substrate. A SiC n type conductivity layer is formed by ion implantation or epitaxial deposition upon the p type layer. The contacting surfaces of the p and n type layers form a junction. A p+ type gate area supported by the n type layer is formed either by the process of ion implantation or the process of depositing and patterning a second p type layer. The **source** and **drain** areas are heavily doped to n+ type conductivity by implanting donor ions in the n type layer.

US PAT NO: 5,506,421 [IMAGE AVAILABLE] L3: 47 of 80

ABSTRACT:
The power metal oxide semiconductor **field effect transistor** (**MOSFET**) has a **drain** region, a channel region, and a **source** region formed of silicon carbide. The **drain** region has a substrate of silicon carbide of a first conductivity type and a **drain**-drift region of silicon carbide adjacent the substrate having the same conductivity type. The channel region is adjacent the **drain**-drift region and has the opposite conductivity type from the **drain**-drift region. The **source** region is adjacent the channel region and has the same conductivity type as the **drain**-drift region. The **MOSFET** also has a gate region having a gate electrode formed on a first portion of the **source** region, a first portion of the channel region, and a first portion of the **drain** region. A **source** electrode is formed on a second portion of the **source** region and a second portion of the channel region. Also, a **drain** electrode is formed on a second portion of the **drain** region.

US PAT NO: 5,486,484 [IMAGE AVAILABLE] L3: 48 of 80

ABSTRACT:
A **MOSFET** device (100) having a silicon carbide substrate (102). A channel region (106) of a first conductivity type and an epitaxial layer (104) of a second conductivity type are located above the silicon carbide substrate (102). First and second **source/drain** regions (118), also of the first conductivity type are located directly within the channel region (106). No well region is placed between the first and second **source/drain** regions (118) and the channel region (106). A gate (120) is separated from the channel region (106) by an insulator layer (110). Insulator layer (110) has a thin portion (114) and a thick portion (116).

US PAT NO: 5,465,249 [IMAGE AVAILABLE] L3: 49 of 80

ABSTRACT:
A random access memory (RAM) cell in 6H-SiC having storage times when all

bias is removed long enough to be considered nonvolatile. The nonvolatile random access memory ([redacted]AM) cell comprises a bit line, [redacted] charge storage device in silicon carbide, and a transistor in silicon carbide connecting the charge storage device to the bit line. The bipolar NVRAM cell has a bipolar transistor with a base region, an emitter region, and a floating collector region, wherein the charge storage device in the bipolar NVRAM is a p-n junction adjacent the floating collector region of the cell. The metal-oxide-semiconductor (MOS) NVRAM has a MOS **field effect transistor** (**MOSFET**) with a channel region, a **source** region, and a **drain** region, wherein the charge storage device in the MOS NVRAM is a MOS capacitor adjacent the **drain** region of the **MOSFET**.

US PAT NO: 5,459,107 [IMAGE AVAILABLE] L3: 50 of 80

ABSTRACT:
A method of obtaining high quality passivation layers on silicon carbide surfaces by oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer on the silicon carbide portion that is substantially free of dopants that would otherwise degrade the electrical integrity of the oxide layer.

US PAT NO: 5,459,089 [IMAGE AVAILABLE] L3: 51 of 80

ABSTRACT:
A high voltage silicon carbide MESFET includes an electric field equalizing region in a monocrystalline silicon carbide substrate at a face thereof, which extends between the **drain** and gate of the MESFET and between the **source** and gate of the MESFET. The region equalizes the electric field between the **drain** and gate and between the **source** and gate to thereby increase the breakdown voltage of the silicon carbide MESFET. The first and second electric field equalizing regions are preferably amorphous silicon carbide regions in the monocrystalline silicon carbide substrate. The amorphous regions are preferably formed by performing a shallow ion implantation of electrically inactive ions such as argon, using the **source** and **drain** electrodes and the metal gate as a mask, at a sufficient dose and energy to amorphize the substrate face. A third amorphous silicon carbide region may be formed at the face, adjacent and surrounding the MESFET to provide edge termination and isolation of the MESFET. The third amorphous, silicon carbide region may be formed during the same shallow implant described above or may be formed in a separate deep implant. The lateral silicon carbide MESFET may be formed in an epitaxial region of second conductivity type on a substrate of first conductivity type, or in an implanted region of second conductivity type in a substrate of first conductivity type.

US PAT NO: 5,449,941 [IMAGE AVAILABLE] L3: 52 of 80

ABSTRACT:
A semiconductor memory device capable of being electrically written and erased comprising a floating gate, wherein, a silicon nitride, silicon oxinitride, aluminum oxide, or silicon carbide film is incorporated between the **drain** region and the floating gate.

US PAT NO: 5,448,081 [IMAGE AVAILABLE] L3: 53 of 80

ABSTRACT:
A **MOSFET** device (100) having a silicon carbide substrate (102). A channel region (106) of a first conductivity type and an epitaxial layer (104) of a second conductivity type are located above the silicon carbide substrate (102). First and second **source/drain** regions (118), also of the first conductivity type are located directly within the channel region (106). No well region is placed between the first and

second **source/drain** regions (118) and the channel region (106). A gate (120) is separated from the channel region (106) by an insulator layer (110). Insulator layer (110) has a thin portion (114) and a thick portion (116).

US PAT NO: 5,441,911 [IMAGE AVAILABLE] L3: 54 of 80

ABSTRACT:
A silicon carbide structure (10) and method capable of using existing silicon wafer fabrication facilities. A silicon wafer (20) is provided which has a first diameter. At least one silicon carbide wafer (30) is provided which has a given width and length (or diameter). The width and length (or diameter) of the silicon carbide wafer (30) are smaller than the diameter of the silicon wafer (20). The silicon wafer (20) and the silicon carbide wafer (30) are then bonded together. The bonding layer (58) may comprise silicon germanium, silicon dioxide, silicate glass or other materials. Structures such as **MOSFET** (62) may be then formed in silicon carbide wafer (30).

US PAT NO: 5,399,883 [IMAGE AVAILABLE] L3: 55 of 80

ABSTRACT:
A high voltage silicon carbide MESFET includes an electric field equalizing region in a monocrystalline silicon carbide substrate at a face thereof, which extends between the **drain** and gate of the MESFET and between the **source** and gate of the MESFET. The region equalizes the electric field between the **drain** and gate and between the **source** and gate to thereby increase the breakdown voltage of the silicon carbide MESFET. The first and second electric field equalizing regions are preferably amorphous silicon carbide regions in the monocrystalline silicon carbide substrate. The amorphous regions are preferably formed by performing a shallow ion implantation of electrically inactive ions such as argon, using the **source** and **drain** electrodes and the metal gate as a mask, at a sufficient dose and energy to amorphize the substrate face. A third amorphous silicon carbide region may be formed at the face, adjacent and surrounding the MESFET to provide edge termination and isolation of the MESFET. The third amorphous silicon carbide region may be formed during the same shallow implant described above or may be formed in a separate deep implant. The lateral silicon carbide MESFET may be formed in an epitaxial region of second conductivity type on a substrate of first conductivity type, or in an implanted region of second conductivity type in a substrate of first conductivity type.

US PAT NO: 5,396,085 [IMAGE AVAILABLE] L3: 56 of 80

ABSTRACT:
A silicon carbide switching device includes a three-terminal interconnected silicon **MOSFET** and silicon carbide MESFET (or JFET) in a composite substrate of silicon and **silicon carbide**. For three terminal operation, the **gate** electrode of the **silicon carbide** MESFET is electrically shorted to the **source** region of the silicon **MOSFET**, and the **source** region of the silicon carbide MESFET is electrically connected to the **drain** of the silicon **MOSFET** in the composite substrate. Accordingly, three-terminal control is provided by the **source** and gate electrode of the silicon **MOSFET** and the **drain** of the silicon carbide MESFET (or JFET). The switching device is designed to be normally-off and therefore blocks positive **drain** biases when the **MOSFET** gate electrode is shorted to the **source** electrode. At low **drain** biases, blocking is provided by the **MOSFET**, which has a nonconductive silicon active region. Higher **drain** biases are supported by the formation of a depletion region in the silicon carbide MESFET (or JFET). To turn-on the device, the gate electrode is biased positive and an inversion layer channel of relatively low resistance is formed in the silicon active region. The channel

electrically connects the **source** of the silicon carbide MESFET (or JFET) with the **source** of the silicon **MOSFET** to thereby turn-on the device when a positive **drain** bias is applied.

US PAT NO: 5,393,999 [IMAGE AVAILABLE] L3: 57 of 80

ABSTRACT:
A **MOSFET** (100) device having a silicon carbide substrate (102) of a first conductivity type. A first epitaxial layer (104) of said first conductivity type and a second epitaxial layer (106) of a second conductivity type are located on a top side of the substrate (102). An insulator layer (108) separates gate electrode (112) from second epitaxial layer (106). A drift region (118) of the first conductivity type is located within the second epitaxial layer (106) on the first side of the gate electrode (112). The drift region has an extension which extends through the second epitaxial layer (106) to the first epitaxial layer (104). **Source** regions (116) and body contact regions (122) are located within the second epitaxial layer (106) on the second side of the gate electrode (112). **Source** regions (116,) and body contact regions (122) are of opposite conductivity type. **Source** electrode (126) electrically connects **source** regions (116) and body contact regions (122). A **drain** electrode (128) is located on a bottom side of the substrate.

US PAT NO: 5,382,822 [IMAGE AVAILABLE] L3: 58 of 80

ABSTRACT:
A **MISFET** (metal-insulator semiconductor **field-effect transistor**) may be used for application at temperatures above 200.degree. C. In particular, leakage currents between the gate electrode (6) and the **drain** (8) are kept at a low level, and a considerable rate of rise in its control characteristic is achieved. An insulating layer (4) of diamond is arranged between the gate electrode (6) and a semiconductor (2) having a larger energy gap than silicon (Si).

US PAT NO: 5,378,642 [IMAGE AVAILABLE] L3: 59 of 80

ABSTRACT:
A silicon carbide (SiC) junction **field effect transistor** (JFET) device is fabricated upon a substrate layer, such as a p type conductivity SiC substrate, using ion implantation for the **source** and **drain** areas. A SiC p type conductivity layer is epitaxially grown on the substrate. A SiC n type conductivity layer is formed by ion implantation or epitaxial deposition upon the p type layer. The contacting surfaces of the p and n type layers form a junction. A p+ type gate area supported by the n type layer is formed either by the process of ion implantation or the process of depositing and patterning a second p type layer. The **source** and **drain** areas are heavily doped to n+ type conductivity by implanting donor ions in the n type layer.

US PAT NO: 5,349,207 [IMAGE AVAILABLE] L3: 60 of 80

ABSTRACT:
A silicon carbide structure (10) and method capable of using existing silicon wafer fabrication facilities. A silicon wafer (20) is provided which has a first diameter. At least one silicon carbide wafer (30) is provided which has a given width and length (or diameter). The width and length (or diameter) of the silicon carbide wafer (30) are smaller than the diameter of the silicon wafer (20). The silicon wafer (20) and the silicon carbide wafer (30) are then bonded together. The bonding layer (58) may comprise silicon germanium, silicon dioxide, silicate glass or other materials. Structures such as **MOSFET** (62) may be then formed in silicon carbide wafer (30).

US PAT NO: 5,338,945 [IMAGE AVAILABLE] L3: 61 of 80

ABSTRACT:
A silicon carbide **field effect transistor** of the present invention includes a base and **source** region each formed by a series of amorphizing, implanting and recrystallizing steps. Moreover, the **drain**, base and **source** regions extend to a face of a monocrystalline silicon carbide substrate and the **source** and base regions comprise substantially monocrystalline silicon carbide formed from recrystallized amorphous silicon carbide, The **source** and base regions also have vertical sidewalls defining the p-n junction between the **source**/base and base/**drain** regions, respectively. The vertical orientation of the sidewalls arises from the respective implantation of electrically inactive ions into the substrate during the amorphizing steps for forming the base region in the **drain** and for forming the **source** region in the base region. The electrically inactive ions are selected from the group consisting of silicon, hydrogen, neon, helium, carbon and argon. A gate and gate insulating region are also provided on the face of the substrate above the base region. By applying an appropriate turn-on base signal to the gate, a channel is created in the base region. The channel region electrically connects the **source** to the **drain**. The **source** and base are also electrically connected by a **source** contact on the face, opposite the portion of the base region wherein the channel is formed.

US PAT NO: 5,323,040 [IMAGE AVAILABLE] L3: 62 of 80

ABSTRACT:
A silicon carbide field effect device includes vertically stacked silicon carbide regions of first conductivity type, extending from a lowermost **drain** region to an uppermost **source** region. In between the **drain** and **source** regions, a drift region and a channel region are provided. The drift region extends adjacent the **drain** region and the channel region extends between the drift region and the **source** region. Control of majority carrier conduction between the **source** and **drain** regions is provided by a plurality of trenches, which extend through the **source** and channel region, and conductive gate electrodes therein. To provide high blocking voltage capability and low on-state resistance, the doping concentration in the drift region is selected to be greater than the doping concentration of the channel region but below the doping concentration of the **drain** and **source** regions. Preferably, the material used for the gate electrodes, the spacing between adjacent trenches and the doping concentration of the channel region are chosen so that the channel region is depleted of majority charge carriers when zero potential bias is applied to the gate electrodes.

US PAT NO: 5,322,802 [IMAGE AVAILABLE] L3: 63 of 80

ABSTRACT:
A silicon carbide field effect transfer of the present invention includes a base and **source** region each formed by a series of amorphizing, implanting and recrystallizing steps. Moreover, the **drain**, base and **source** regions extend to a face of a monocrystalline silicon carbide substrate and the **source** and base regions comprise substantially monocrystalline silicon carbide formed from recrystallized amorphous silicon carbide. The **source** and base regions also have vertical sidewalls defining the p-n junction between the **source**/base and base/**drain** regions, respectively. The vertical orientation of the sidewalls arises from the respective implantation of electrically inactive ions into the substrate during the amorphizing steps for forming the base region in the **drain** and for forming the **source** region in the base region. The electrically inactive ions are selected from the group consisting of silicon, hydrogen, neon, helium, carbon and argon. A gate and gate insulating region are also provided on the face of the substrate above the base region. By applying an appropriate turn-on bias

signal to the gate, a channel is created in the base region. The channel region electrically connects the **source** to the **drain**. The **source** and base are also electrically connected by a **source** contact on the face, opposite the portion of the base region wherein the channel is formed.

US PAT NO: 5,309,007 [IMAGE AVAILABLE] L3: 64 of 80

ABSTRACT:
A **field effect transistor** having a buried gate, and one or more gates disposed along the channel between the **source** and **drain**, which cooperate to cause the electric field within the channel along its length to be more uniform, and have a lower field maximum. The geometry and/or doping of the channel can be varied to selectively vary the channel resistivity along its length, which also makes the field more uniform. Because of the more uniform field, electrons are exposed to a higher field strength nearer the **source**, and are accelerated to higher velocities more quickly, reducing the response time and increasing the frequency range of the transistor. Because the peak field is reduced, the transistor can carry more power without reaching breakdown potential within the channel.

US PAT NO: 5,307,305 [IMAGE AVAILABLE] L3: 65 of 80

ABSTRACT:
A semiconductor device having a **field effect transistor** in which a silicon carbide layer and a ferroelectric film are stacked in this order on the surface of a silicon substrate and the ferroelectric film is used as a gate insulation film. A channel between a **source** and a **drain** is formed in the silicon carbide layer. A metal or oxygen contained in a ferroelectric material is difficult to diffuse in silicon carbide. Therefore, the silicon carbide layer is not eroded in the case of heat treatment after forming the ferroelectric film. Therefore, good **FET** characteristics is obtained.

US PAT NO: 5,270,554 [IMAGE AVAILABLE] L3: 66 of 80

ABSTRACT:
A high power, high frequency, metal-semiconductor **field-effect transistor** comprises a bulk single crystal silicon carbide substrate, an optional first epitaxial layer of p-type conductivity silicon carbide formed upon the substrate, and a second epitaxial layer of n-type conductivity silicon carbide formed upon the first epitaxial layer. The second epitaxial layer has two separate well regions therein that are respectively defined by higher carrier concentrations of n-type dopant ions than are present in the remainder of the second epitaxial layer. Ohmic contacts are positioned upon the wells for respectively defining one of the well regions as the **source** and the other as the **drain**. A Schottky metal contact is positioned upon a portion of the second epitaxial layer that is between the ohmic contacts and thereby between the **source** and **drain** for forming an active channel in the second epitaxial layer when a bias is applied to the Schottky contact.

US PAT NO: 5,264,713 [IMAGE AVAILABLE] L3: 67 of 80

ABSTRACT:
A junction **field-effect transistor** is disclosed that comprises a bulk single crystal silicon carbide substrate having respective first and second surfaces opposite one another, the substrate having a single polytype and having a concentration of suitable dopant atoms so as to make the substrate a first conductivity type. A first epitaxial layer of silicon carbide is formed on the first surface of the substrate, and having a concentration of suitable dopant atoms that give the first epitaxial layer the first conductivity type. A second epitaxial layer of silicon carbide is formed on the first epitaxial layer, the

second epitaxial layer having a concentration of suitable dopant atoms to give the second epitaxial layer a second conductivity type opposite from the first conductivity type. A higher conductivity region of silicon carbide is formed on the second epitaxial layer, A trench is formed in the second epitaxial layer and higher conductivity region extending entirely through the higher conductivity region and partially into the second epitaxial layer toward the first surface of the substrate for defining a gate region in the second epitaxial layer between the trench and the first epitaxial layer. The trench divides the second epitaxial layer and higher conductivity region into respective first and second regions with the trench therebetween.

US PAT NO: 5,229,625 [IMAGE AVAILABLE] L3: 68 of 80

ABSTRACT:
The semiconductor device somprises a silicon substrate, a boron-doped high resistant silicon carbide layer formed on said silicon substrate and a silicon carbide layer formed on said high resistant silicon carbide layer.

US PAT NO: 5,216,264 [IMAGE AVAILABLE] L3: 69 of 80

ABSTRACT:
A silicon carbide **field-effect transistor** is disclosed which includes an MOS structure composed successively of a **silicon carbide** layer, a **gate** insulator film, and a gate electrode. The **field-effect transistor** has **source** and **drain** regions formed in the silicon carbide layer, between which the MOS structure is disposed, wherein at least one of the **source** and **drain** regions is formed by the use of a Schottky contact on the silicon carbide layer.

US PAT NO: 5,170,231 [IMAGE AVAILABLE] L3: 70 of 80

ABSTRACT:
A silicon carbide **field-effect transistor** is provided which includes a semiconductor substrate, a channel formation layer of silicon carbide formed above the substrate, **source** and **drain** regions provided in contact with the channel formation layer, a gate insulator disposed between the **source** and **drain** regions, and a gate electrode formed on the gate insulator, wherein a first contact between the channel formation layer and the **drain** region exhibits different electric characteristics from those of a second contact between the channel formation layer and the **source** region. Also provided is a method for producing such a silicon carbide **field-effect transistor**.

US PAT NO: 5,135,885 [IMAGE AVAILABLE] L3: 71 of 80

ABSTRACT:
A method of manufacturing a semiconductor device comprises the steps of (i) forming a SiC monocrystal layer over the entire surface of a semiconductor substrate; (ii) forming a boron ion implanted layer, which is substantially a thin film, by implanting a specified amount of boron ions in the surface region of the SiC monocrystal layer; and (iii) forming a high resistance SiC monocrystal layer of a thin film by subjecting the boron ion implanted layer to heat treatment; whereby the high resistance SiC monocrystal layer can be function at least as an electric insulating layer.

US PAT NO: 5,124,779 [IMAGE AVAILABLE] L3: 72 of 80

ABSTRACT:
A silicon carbide semiconductor device is disclosed which includes a silicon carbide single-crystal layer and at least one ohmic electrode in contact with the silicon carbide single-crystal layer, wherein the ohmic

electrode is made of a titanium-aluminum alloy. Also disclosed is a method of producing th[redacted]ilicon carbide semiconductor d[redacted]ce.

US PAT NO: 4,980,303 [IMAGE AVAILABLE] L3: 73 of 80

ABSTRACT:
With a trend toward higher operation speed and higher gain of a Bi-MIS semiconductor device, wherein a bipolar transistor and a MIS **FET** are formed on the same silicon substrate, a wide bandgap material such as silicon carbide or micro-crystalline silicon is utilized as an emitter material of the bipolar transistor and further a gate electrode of the MIS **FET** is simultaneously formed using the same wide bandgap material. By applying the above method in the manufacturing of the Bi-MIS semiconductor device, a high amplification factor of the bipolar transistor and a high cutoff frequency of the MIS **FET** thereof can be easily obtained without additional processes.

US PAT NO: 4,966,860 [IMAGE AVAILABLE] L3: 74 of 80

ABSTRACT:
A process for producing a SiC semiconductor device comprising growing a single-crystal film of SiC on a single-crystal substrate of Si and forming the structure of semiconductor device such as diodes, transistors, etc., on said SiC single-crystal film, thereby obtaining a SiC semiconductor device on a commercial scale.

US PAT NO: 4,929,985 [IMAGE AVAILABLE] L3: 75 of 80

ABSTRACT:
A compound semiconductor device comprises: a III-V group compound semiconductor substrate and a Schottky junction electrode of p-type amorphous silicon carbide (a-SiC) layer provided on the III-V group compound semiconductor substrate and an amorphous silicon-germanium-boron (a-Si-Ge-B) layer provided on the p-type amorphous silicon carbide layer.

US PAT NO: 4,897,710 [IMAGE AVAILABLE] L3: 76 of 80

ABSTRACT:
The semiconductor device comprises a silicon substrate, a boron-doped high resistant silicon carbide layer that is formed on the silicon substrate and a silicon carbide layer formed on the high resistant silicon carbide layer. The silicon carbide layer that is formed on the high resistant silicon carbide layer provides an electrical insulation for the device so that improved device characteristics are obtained.

US PAT NO: 4,762,806 [IMAGE AVAILABLE] L3: 77 of 80

ABSTRACT:
A process for producing a SiC semiconductor device comprising growing a single-crystal film of SiC on a single-crystal substrate of Si and forming the structure of semiconductor device such as diodes, transistors, etc., on said SiC single-crystal film, thereby obtaining a SiC semiconductor device on a commercial scale.

US PAT NO: 4,757,028 [IMAGE AVAILABLE] L3: 78 of 80

ABSTRACT:
A silicon carbide layer(s) is provided on a silicon substrate. If necessary, a desired pattern of the silicon carbide layer(s) is allowed to remain, while the other portion(s) is embedded with SiO.sub.2. If necessary, the silicon carbide layer(s) may be constituted of a barrier layer and a device-forming layer. A layer capable of easily forming an insulating layer, such as a polycrystalline silicon layer, is provided on the silicon carbide layer to form first electrodes, followed by insulation of the surface, such as oxidation of the surfaces of the first

electrodes and the silicon carbide layer. Second electrodes are further formed in self alignment by utilizing the insulating layer of the surface of the first electrodes. This process is useful in preparation of a silicon carbide device capable of operation at high temperatures.

US PAT NO: 4,513,309 [IMAGE AVAILABLE] L3: 79 of 80

ABSTRACT:
A complementary metal oxide semiconductor (CMOS) circuit is described incorporating Schottky barrier diodes in parallel with the **source** or **drain** of either the P or N channel transistors to reduce the minority current injected into the body at times the **source** or **drain** of either the N or P channel transistors are forward biased. The Schottky diode may be fabricated by making enlarged openings exposing both the body (substrate) and **drain** or **source** region and by using a metallization which may form an ohmic contact with the **drain** or **source** region and at the same time for a Schottky diode with the substrate. By incorporating Schottky barrier diodes parallel to the **drain** or **source** the P and N-type transistors are not current limited by the barrier height of only a Schottky diode acting as the **source** and at the same time minority current is not injected into the substrate or body at times the **drain** or **source** is forward biased. An input and output protection network is also described incorporating Schottky diodes.

US PAT NO: 4,507,673 [IMAGE AVAILABLE] L3: 80 of 80

ABSTRACT:
A semiconductor memory device is disclosed which comprises:
a semiconductor substrate of n conductivity type;
source and **drain** regions of p.sup.+ conductivity type formed in the substrate;
a first gate insulation film of silicon dioxide (SiO.sub.2) formed on the substrate; and
a second **gate** insulation film of **silicon carbide** (**SiC**) formed on the first **gate** insulation film.

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  * PATENT OFFICE ABSTRACT (JPOABS) FILE.  NEW RECORDS ARE NOT *
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          7800 MOSFET?
         38421 FET?
        124308 FIELD
        180521 EFFECT
        101973 TRANSISTOR?
          7937 FIELD-EFFECT-TRANSISTOR?
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                (FIELD(W)EFFECT(W)TRANSISTOR?)
          1410 MISFET?
          6257 SIC
         80962 SILICON
         14738 CARBIDE?
          5499 SILICON-CARBIDE?
                 (SILICON(W)CARBIDE?)
        127175 GATE?
            10 (SIC OR SILICON-CARBIDE?)(5W)GATE?
        127175 GATE?
          6257 SIC
         80962 SILICON
         14738 CARBIDE?
          5499 SILICON-CARBIDE?
                 (SILICON(W)CARBIDE?)
            12 GATE?(5W)(SIC OR SILICON-CARBIDE?)
L4           9 L1 AND ((SIC OR SILICON-CARBIDE?)(5W)GATE? OR GATE?(5W)(SIC
 OR
                 SILICON-CARBIDE?))

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08-336238                                                L4: 1 of 9


ABSTRACT:

 PURPOSE: To obtain a power supply system for vehicle in which the output
from an AC electric rotating machine can be taken out efficiently while
ensuring low rectification loss even in the low speed rotational region
without requiring an extra surge absorption circuit by utilizing an
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SiC-**MOSFET** effectively and contriving the conduction system therefor.

CONSTITUTION: Based on the phase of voltage generated from an AC generator 10, a microcomputer 50 determines an interval for feeding a battery Ba with the voltage obtained by rectifying the voltage generated from each armature coil thus determining the timing for short-circuiting each armature coil at a predetermined duty. Based on the determination results, a logic **gate** circuit 40 controls each **SiC-MOSFET** such that the boosting of each generated voltage due to open/short circuit of each armature coil and the output of rectified voltage to the battery Ba are carried out periodically through selective conduction of SiC-**MOSFETs** in a rectifier 20.

07-263687 L4: 2 of 9

ABSTRACT:

PURPOSE: To lower the temperature dependency of an SiC-**MOSFET** by increasing the magnitude of a gate input signal in accordance with the temperature rise of an element, which signal is for maintaining the ON-state of an insulated gate **field effect transistor** in the linear region of an operating region.

CONSTITUTION: A voltage monitoring circuit 12 changes the frequency of an output pulse signal, according to the signal from a temperature monitoring circuit 193 which monitors the temperature of an SiC-**MOSFET** 191 through a temperature sensor 192, and controls the voltage of a capacitor 17. A switching control circuit 194 executes the switching operation of the SiC- **MOSFET** 191 through a transistor circuit 19, which is connected with a capacitor 17. Hence the voltage level of a **gate** input signal 10 of the **SiC-MOSFET** 191 is controlled in accordance with the temperature of the SiC-**MOSFET** 191. Since the control method wherein the gate voltage is made large in accordance with the temperature is adopted, the temperature dependency of an element can be lowered.

07-142732 L4: 3 of 9

ABSTRACT:

PURPOSE: To improve the mutual conductance of an insulated-gate **field effect transistor** formed in an active layer of silicon carbide.

CONSTITUTION: An n-type or p-type silicon carbide potential barrier layer 2 is epitaxially grown between a single-crystal silicon wafer 1 and a p-type or n-type active layer of **silicon carbide** 3. An insulated-**gate field effect transistor** functions using this p-type or n-type silicon carbide layer 3 as a channel layer. An n-type or p-type silicon carbide forms a potential barrier against holes or electrons, and the supply of holes or electrons to the channel is blocked. Accordingly, the conductivity of the channel becomes larger, and the mutual conductance is improved.

07-115191 L4: 4 of 9

ABSTRACT:

PURPOSE: To improve the performance of a diamond **FET** by a method wherein a diamond layer which has high impurity concentration doped surface parts and source and drain regions which are separated from each other with a certain distance and a **gate** composed of a **silicon carbide** layer are provided and the **gate** is placed on an active channel region.

CONSTITUTION: A diamond layer 12 formed on a support substrate 13 has a drain region 16 and a source region 15 which are horizontally separated from each other and an active channel region 14 spread between the source region 15 and the drain region 16. The surface parts 15a and 16a of the source region 15 and the drain region 16 are doped with high concentration impurities. Further, contact layers 15b and 16b on the surface parts 15a and 15b are composed of double-layer structures of titanium and gold or titanium carbide and gold. A silicon carbide layer 17 which is to be the gate of an **FET** 10 is formed on the diamond layer 12 which is the surface layer on the active channel region 14 and, further, between the surface parts 15a and 16a. A conductive contact layer17a is formed on the silicon carbide layer 17.

05-160149 L4: 5 of 9

ABSTRACT:

PURPOSE:To obtain improved **FET** characteristics by using a region near a surface of a silicon carbide layer as a channel region without diffusing a metal and oxygen within a ferroelectric film into a **silicon carbide** layer by forming a **gate** electrode on the **silicon carbide** layer which is formed on the substrate through the ferroelectric film, etc.

CONSTITUTION:A title item is provided with a conductive type silicon carbide layer 14 which is formed on a surface of a substrate 11 and a pair of semiconductor thin films 13A and 13B which are formed on a surface of the substrate 11 so that they contact the silicon carbide layer 14 at a different position and become source/drain. Furthermore, it is provided with a ferroelectric film 15 which is formed in lamination on the **silicon carbide** layer 14 and a **gate** electrode 16 which is formed on the ferroelectric film 15. For example, the P-type silicon carbide layer 14 is formed on a surface of the P-type silicon substrate 11, a silicon oxide film 12 is formed on regions on both sides, and then a pair of N.sup.+-type polysilicon films 13A and 13B are formed on it.

03-222367 L4: 6 of 9

ABSTRACT:

PURPOSE:To prevent a transistor of this design from deteriorating in characteristics by a method wherein a **gate** electrode of **silicon carbide** layer is formed on a one conductivity type semiconductor substrate through the intermediary of an insulating layer, and opposite conductivity type impurities are introduced into the exposed part of the substrate on the sides to form a source and drain region.

CONSTITUTION:An isolation insulating layer 2 is formed on an N-type silicon substrate 1, a gate oxide film 3 is formed on the exposed surface of the substrate 1, and an SiC film 4 is formed on the entire surface. Then, a resist mask 5 is formed, and a plasma etching is carried out onto the exposed **SiC** film 4 to form a **gate** electrode 41, and then the

exposed gate oxide film 2 is also etched to make the silicon substrate 1 exposed. Then, the resist mask 5 is removed, the surface of the silicon substrate 1 is treated to form an oxide film 32 on the exposed surface of the substrate 1, and a source region and drain region 6 of P-type are formed on the substrate 1. In succession, the oxide film 32 is removed, an interlaminar insulating layer 7 of phospho-silicate glass is formed on the surface of the silicon substrate 1, a contact hole 71 is formed, and a wiring 8 connected to the source and the drain regions 6 is formed to complete a transistor of this design.

03-136278 L4: 7 of 9

ABSTRACT:

PURPOSE:To enable the manufacture of a silicon carbide **field-effect transistor** adapted for mass production in an industrial scale taking productivity into consideration by a method wherein a first conductivity type silicon carbide single crystal film is grown on a silicon substrate, and then a second conductivity type region is selectively formed on the first conductivity type single crystal film to form a source and a drain region.

CONSTITUTION:A first conductivity type silicon carbide single crystal film 12 is made to grow on a silicon substrate 11, and a second conductivity type region is selectively formed on the film 12 to form a source region 13 and a drain region 14. Then, an insulating film 15 is formed on the film 12, and the insulating film 15 formed on the source and the drain region, 13 and 14, is selectively removed. A source and a drain electrode, 16 and 17, are formed on the source region 13 and the drain region 14 respectively, and a gate electrode 18 is formed on the insulating film 15 left unremoved. For instance, a very thin silicon carbide polycrystalline layer is formed on the N-type single crystal substrate 11 through a low temperature CVD method, in succession the temperature of the silicon substrate 11 is made to rise to 1350.degree.C to enable a P-type silicon carbide single crystal film 12 to grow on the silicon carbide polycrystalline layer as thick as a few .mu.m through a CVD method.

01-86547 L4: 8 of 9

ABSTRACT:

PURPOSE:To decrease the number of processes, and to realize an element having excellent performance, stability and reliability by constructing an Si semiconductor element by using a pattern film being employed for selectively growing a single crystal SiC film and composed of a high melting-point material as a mask and a surface protective film as it is without being peeled.

CONSTITUTION:A gate electrode 9, a source electrode 10 and a drain electrode 11 are formed onto an N-type single crystal SiC film 4, thus constructing an **SiC Schottky gate type field-effect transistor**. A window is bored to an SiO.sub.2 pattern film 2a, and an ohmic electrode 12 to a P-type Si layer 7 and an ohmic electrode 13 to an N-type Si layer 8 are shaped, thus constituting an Si P-N junction diode. Consequently, an SiC semiconductor element and an Si semiconductor element can be built to the same single crystal Si substrate 1. An SiO.sub.2 pattern film used for selectively growing the single crystal SiC film can be utilized as a mask for manufacturing the Si semiconductor element and a surface protective film in the Si semiconductor element after manufacture as it is.

63-289960 L4: 9 of 9

ABSTRACT:

PURPOSE:To obtain a new type of a **field effect transistor** higher in operational speed and integration as compared with a conventional MOS **FET** by a method wherein a gate electrode is provided through intermediary of a single crystal silicon carbide film epitaxially grown on a substrate.

CONSTITUTION:A carrier in a silicon substrate adjacent to the interface between a silicon substrate 1 and a silicon carbide film 2 is controlled by applying voltage through the single crystal silicon carbide film 2 which is formed and bonded onto a silicon substrate 1. For instance, an element isolation film 6 is provided on the p-type silicon substrate 1 with a face orientation (100) and an undoped SiC single crystal film 2 is epitaxially grown through the vacuum vapour phase growth on an Si face on which an element is to be formed. Polycrystalline Si is deposited thereon, and then patterning is performed to form a **gate** electrode structure consisting of the **SiC** film 2 with a channel 1 .mu.m in length and a gate electrode 3. Next, As.sup.+ is ion-implanted through the said electrode 3 as a mask and heat treatment is performed for activation, and thus a source region 4 and a drain region 5 are formed.